AMENDMENTS TO THE CLAIMS

1-20 (Canceled)

21. (Previously presented) A memory cell intermediate structure, comprising:

a substrate;

a first conductor formed on said substrate;

an insulator formed on said first conductor, at least one via formed within said insulator and extending to said first conductor;

a metallic material formed in said at least one via; and

a flowable oxide material localized within said at least one via and over said metallic material within said via such that a top surface of said flowable oxide material is below a top surface of said insulator.

22. (Previously presented) The memory cell intermediate structure of claim 21, wherein said metallic material comprises silver.

23. (cancelled)

24. (Previously presented) The memory cell intermediate structure of claim 21, wherein said metallic material is deposited on a surface of said insulator.

25. (Currently amended) A ~~programmable conductor random access memory~~ memory cell intermediate structure, comprising:

a metallic material formed on a surface of an insulating layer and within and over a bottom of a via in said insulating layer; and

a flowable oxide material localized within said via and over said metallic material within said via such that a top surface of said flowable oxide material is below a top surface of said insulating layer.

26. (Currently amended) The ~~programmable conductor random access memory~~ memory cell intermediate structure of claim 25, wherein said metallic material comprises silver.

27. (cancelled)

28. (Currently amended) The ~~programmable conductor random access memory~~ memory cell intermediate structure of claim 25, wherein said flowable oxide comprises silicon oxide.

29. (Currently amended) The ~~programmable conductor random access memory~~ memory cell intermediate structure of claim 28, wherein said silicon oxide is in a flowable form in a temperature range of 50° C to 90° C.

30. (New) The memory cell intermediate structure of claim 25, wherein said intermediate structure is a programmable conductor random access memory.